In the Specification:

Please replace the paragraph beginning at page 10, line 19, with the following rewritten paragraph:

-- The prior art top view of Figure 6 shows a portion of the features of the FC1 signal redistribution layer 21 in Figure 1. As previously mentioned, signal pads 37 on the FC2 layer of Figure 5 are connected to signal pads 37 on the FC1 layer of Figure 6 by conductive vias. At this level, the remainder of the signal 37 pads escape off chip. As shown, the only region with enough open space to accommodate power distribution PTHs, underlying PTH pads 43, is region 25. This is due to the fact that the space in regions 29 and 31 are taken up with signal pads 37 and signal escape wires 39. --